

EAST - [879841b.1]

File View Edit Tools Window Help

BRS: optimiz\$5 near9 timing near9 cell

Pending

Active

L3: (0) variable near9 depth and 12

L7: (8) (variable same form) and 12

L8: (8) (variable near9 form) and 12

L10: (0) variable same depth and 12

L11: (8) variable and depth and 12

L12: (14) ((select\$4 near9 logic near9 operat\$3) and (fun

L13: (33) podkolzin-alexander-s.inv.

Failed

US-PGPUB,USPAT,EPQ

Plural

Highlight all hit terms initially

Default operator

OR

((select\$4 near9 logic near9 operat\$3) and (function\$3 same logic same cell) and (select\$4 near9 input) and (predetermin\$4 near9 input)) and (optimiz\$5 same timing)

BRS form

ISIR form

Image

Text

HTML

	U	I	Document ID	Iss	Title	Current	Ci
1	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 20040210857	20	Method for optimal driver selection	716/2	71
2	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 20030204822	20	Digital logic optimization using selection operators	716/2	71
3	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 20030200510	20	Digital circuits using universal logic gates	716/1	
4	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 20030177457	20	Optimization of digital designs	716/3	71
5	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 20030149953	20	Integrated circuit cell library	716/17	
6	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 20030126579	20	Digital design using selection operations	716/18	
7	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6792589	B2 20	Digital design using selection operations	716/18	71
8	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6779158	B2 20	Digital logic optimization using selection operators	716/3	71
9	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6779156	B2 20	Digital circuits using universal logic gates	716/1	71
10	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6754877	B1 20	Method for optimal driver selection	716/2	71
11	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6701507	B1 20	Method for determining a zero-skew buffer insertion point	716/10	32
12	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6701506	B1 20	Method for match delay buffer insertion	716/10	32
13	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6698006	B1 20	Method for balanced-delay clock tree insertion	716/10	71
14	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	US 6591407	B1 20	Method and apparatus for interconnect-driven optimization of	716/10	71

☒ Hits

☐ Details

☒ HTML

Ready

REIN